DATA SHEET

TDA8005A
Low-power (3 V/5 V) smart card coupler

Preliminary specification
File under Integrated Circuits, IC17

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Philips
Semiconductors

PHILIPS

Low-power (3 V/5 V) smart card coupler TDA8005A

FEATURES

- Smart card supply (5 and 3 V ±5%, 20 mA maximum with controlled rise and fall times)
- Smart card clock generation (up to 8 MHz), with two times synchronous frequency doubling
- Clock STOP HIGH, clock STOP LOW or 1.25 MHz (from internal oscillator) for cards power-down mode
- Specific UART on I/O for automatic direct/inverse convention settings and error management at character level
- Automatic activation and deactivation sequences through an independent sequencer
- Supports the protocol T = 0 in accordance with ISO 7816 GSM11.11 requirements (Global System for Mobile communication); approved for Final GSM11.11 Test Approval (FTA)
- Several analog options are available for different applications: doubler or tripler DC-to-DC converter, card presence, active HIGH or LOW, threshold voltage supervisor, etc.
- Overloads and take-off protections
- Current limitations in the event of short-circuit
- Special circuitry for killing spikes during power-on or off
- Supply supervisor
- Step-up converter (supply voltage from 2.5 to 6 V)
- Power-down and sleep mode for low power consumption
- Enhanced ElectroStatic Discharge (ESD) protections on card side (6 kV minimum)
- Control and communication through a standard RS232 full-duplex interface
- Optional additional I/O ports for:
  - keyboard
  - LEDs
  - display
  - etc.
- P80CL51 microcontroller core with 4-kbyte ROM and 256-byte RAM.

APPLICATIONS

- Portable smart card readers for protocol T = 0
- GSM mobile phones.

GENERAL DESCRIPTION

The TDA8005A is a low-cost card interface for portable smart card readers. Controlled through a standard serial interface, it takes care of all ISO 7816 and GSM11.11 requirements for both 5 and 3 V cards. It gives the card and the set a very high level of security, due to its special hardware against ESD, short-circuiting, power failure, etc. Its integrated step-up converter allows operation within a supply voltage range of 2.5 to 6 V.

The very low power consumption in power-down and sleep modes saves battery power.

Development tools, application report and support (hardware and software) are available.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8005AG	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
TDA8005AH	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

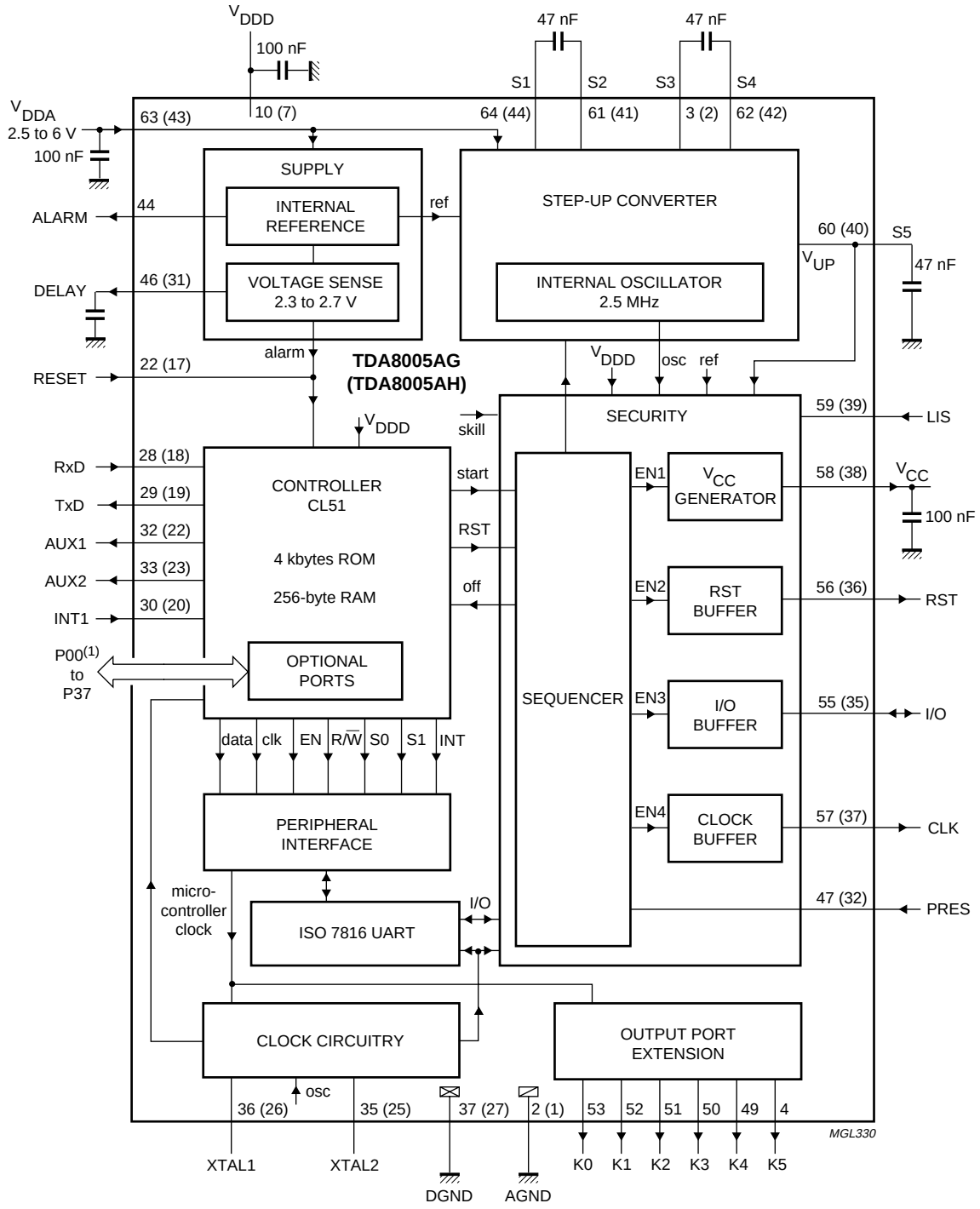
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	doubler and tripler option	2.5	–	6.0	V
$I_{DD(pd)}$	supply current in power-down mode	V_{DD} = 5 V; card inactive	–	100	–	µA
$I_{DD(sm)}$	supply current in sleep mode	card powered but clock stopped; no load				
		doubler option	–	500	–	µA
		tripler option	–	700	–	µA
$I_{DD(om)}$	supply current in operating mode	unloaded; f_{XTAL} = 13 MHz; $f_{\mu C}$ = 6.5 MHz; f_{card} = 3.25 MHz	–	5.5	–	mA
V_{CC}	card supply voltage	5 V card				
		no load	4.85	5.05	5.25	V
		static load	4.75	5.0	5.25	V
		dynamic load on 200 nF capacitor	4.5	–	5.4	V
		3 V card				
		no load	2.9	3.03	3.15	V
		static load	2.79	3	3.21	V
		dynamic load on 200 nF capacitor	2.75	–	3.25	V
I_{CC}	card supply current	operating	–	–	20	mA
		limitation	–	–	note 1	mA
SR	slew rate on V_{CC} (rise and fall)	maximum load capacitor 250 nF (including typical 200 nF decoupling)	0.04	0.1	0.16	V/µs
t_{de}	deactivation sequence duration		–	–	225	µs
t_{act}	activation sequence duration		–	–	150	µs
f_{XTAL}	crystal frequency		2	–	16	MHz
T_{amb}	operating ambient temperature		–25	–	+85	°C

Note

1. See Table 3 for mask options.

BLOCK DIAGRAM



Pin numbers in parenthesis represent the TDA8005AH.

(1) For details see Chapter “Pinning” and Table 3.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	LQFP64	QFP44	
n.c.	1	–	not connected
AGND	2	1	analog ground
S3	3	2	contact 3 for the step-up converter
K5	4	–	output port from port extension
P03	5	3	general purpose I/O port (connected to port P03)
P02	6	4	general purpose I/O port (connected to port P02)
P01	7	5	general purpose I/O port (connected to port P01)
n.c.	8	–	not connected
P00	9	6	general purpose I/O port (connected to port P00)
V_{DDD}	10	7	digital supply voltage
n.c.	11	–	not connected
TEST1	12	8	test pin 1 (connected to port P10; must be left open-circuit in the application)
P11	13	9	general purpose I/O port or interrupt (connected to port P11)
P12	14	10	general purpose I/O port or interrupt (connected to port P12)
P13	15	11	general purpose I/O port or interrupt (connected to port P13)
P14	16	12	general purpose I/O port or interrupt (connected to port P14)
n.c.	17	–	not connected
P15	18	13	general purpose I/O port or interrupt (connected to port P15)
P16	19	14	general purpose I/O port or interrupt (connected to port P16)
TEST2	20	15	test pin 2 (connected to PSEN; must be left open-circuit in the application)
P17	21	16	general purpose I/O port or interrupt (connected to port P17)
RESET	22	17	input for resetting the microcontroller (active HIGH)
n.c.	23	–	not connected
n.c.	24	–	not connected
n.c.	25	–	not connected
n.c.	26	–	not connected
n.c.	27	–	not connected
RxD	28	18	serial interface receive line
TxD	29	19	serial interface transmit line
INT1	30	20	general purpose I/O port or interrupt (connected to port P33)
T0	31	21	general purpose I/O port (connected to port P34)
AUX1	32	22	push-pull auxiliary output (±5 mA; connected to timer T1 e.g. port P35)
AUX2	33	23	push-pull auxiliary output (±5 mA; connected to timer; port P36)
P37	34	24	general purpose I/O port (connected to port P37)
XTAL2	35	25	crystal connection
XTAL1	36	26	crystal connection or external clock input
DGND	37	27	digital ground
n.c.	38	–	not connected

SYMBOL	PIN		DESCRIPTION
	LQFP64	QFP44	
n.c.	39	–	not connected
P20	40	28	general purpose I/O port (connected to port P20)
P21	41	–	general purpose I/O port (connected to port P21)
P22	42	29	general purpose I/O port (connected to port P22)
P23	43	30	general purpose I/O port (connected to port P23)
ALARM	44	–	open-drain output for power-on reset (active HIGH or LOW by mask option)
n.c.	45	–	not connected
DELAY	46	31	external capacitor connection for delayed reset signal
PRES	47	32	card presence contact input (active HIGH or LOW by mask option)
TEST3	48	33	test pin 3 (must be left open-circuit in the application)
K4	49	–	output port from port extension
K3	50	–	output port from port extension
K2	51	–	output port from port extension
K1	52	–	output port from port extension
K0	53	–	output port from port extension
TEST4	54	34	test pin 4 (must be left open-circuit in the application)
I/O	55	35	data line to/from the card (ISO C7 contact)
RST	56	36	card reset output (ISO C2 contact)
CLK	57	37	clock output to the card (ISO C3 contact)
V_{CC}	58	38	card supply output voltage (ISO C1 contact)
LIS	59	39	supply for low-impedance on cards contacts
S5	60	40	contact 5 for the step-up converter
S2	61	41	contact 2 for the step-up converter
S4	62	42	contact 4 for the step-up converter
V_{DDA}	63	43	analog supply voltage
S1	64	44	contact 1 for the step-up converter

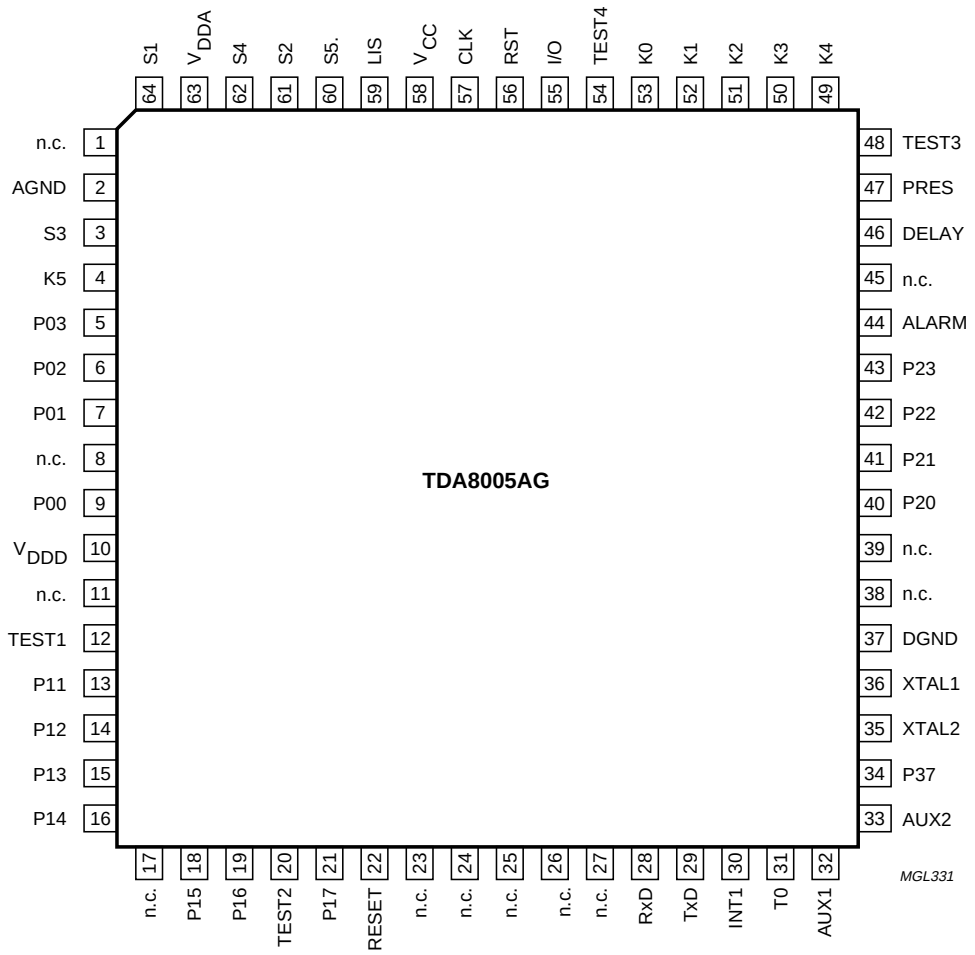


Fig.2 Pin configuration (LQFP64).

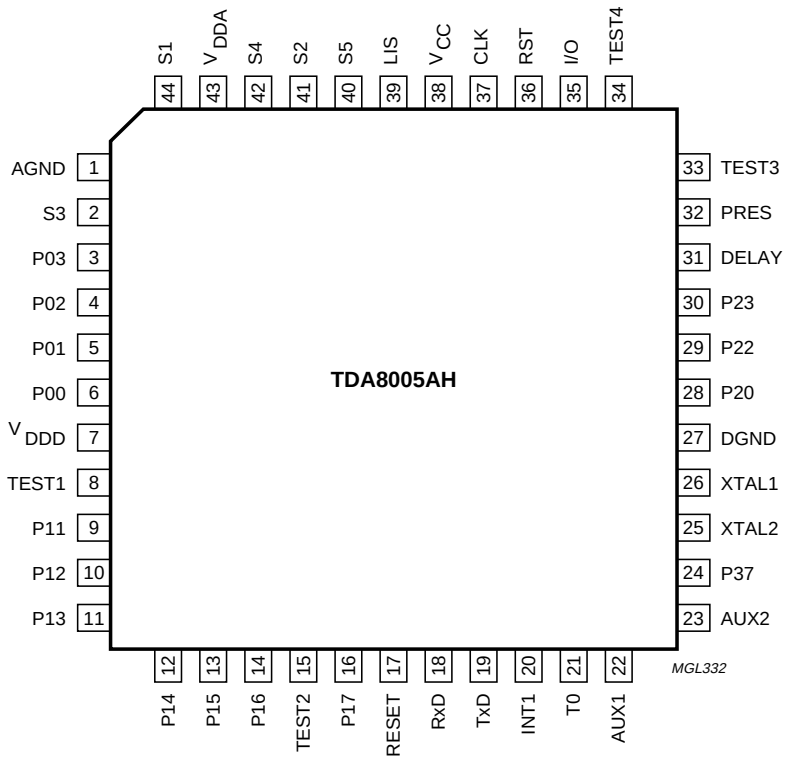


Fig.3 Pin configuration (QFP44).

FUNCTIONAL DESCRIPTION

Microcontroller

The microcontroller is a P80CL51 with 256 bytes of RAM instead of 128. The baud rate of the UART has been multiplied by four in modes 1, 2 and 3. This means that the division factor of 32 in the formula is replaced by 8 in both reception and transmission mode and that in the reception modes only four samples per bit are taken with decision on the majority of samples 2, 3 and 4; the delay counter has been reduced from 1536 to 24 as well.

Remark: this has an impact when getting out of power-down mode. It is recommended to switch to internal clock before entering power-down mode.

All the other functions remain unchanged. Refer to the P80CL51 data sheet for any further information. Internal ports INT0 (P32), P10, P04 to P07 and P24 to P27 are used for controlling the smart card interface.

Mode 0 is unchanged. The baud rate for modes 1 and 3 is:

$$\frac{2^{SMOD}}{8} \times \frac{f_{clk}}{12 \times (256 - TH1)}$$

The baud rate for mode 2 is:

$$\frac{2^{SMOD}}{16} \times f_{clk}$$

For mode 3 timing see Table 1.

Table 1 Mode 3 timing

BAUD RATE	f_{clk} = 6.5 MHz; V_{DD} = 5 V		f_{clk} = 3.25 MHz; V_{DD} = 5 or 3 V	
	SMOD	TH1	SMOD	TH1
135416	1	255	–	–
67708	0	255	1	255
45139	1	253	–	–
33854	0	254	0	255
27083	1	251	–	–
22569	0	253	1	253
16927	–	–	0	254
13542	–	–	1	251
11285	0	250	0	253

Supply

The circuit operates within a supply voltage range of 2.5 to 6 V. The supply pins are V_{DDD}, V_{DDA}, DGND and AGND. Pins V_{DDA} and AGND supply the analog drivers to the card and have to be externally decoupled because of the large current spikes that the card and the step-up converter can create. An integrated spike killer ensures the contacts to the card remain inactive during power-up or power-down. An internal voltage reference is generated which is used within the step-up converter, the voltage supervisor and the V_{CC} generator.

The voltage supervisor generates an internal alarm pulse, whose length is defined by an external capacitor tied to the DELAY pin, when V_{DDD} is too low to ensure proper operation (1 ms per 1 nF typical). This pulse is used as a reset pulse by the controller, in parallel with an external reset input, which can be tied to the system controller.

It is also used in order to either block any spurious card contacts during controllers reset, or to force an automatic deactivation of the contacts in the event of supply dropout; see Sections “Activation sequence” and “Deactivation sequence”.

In the 64 pin version, this reset pulse is output to the open drain ALARM pin, which may be selected active HIGH or active LOW by mask option and may be used as a reset pulse for other devices within the application.

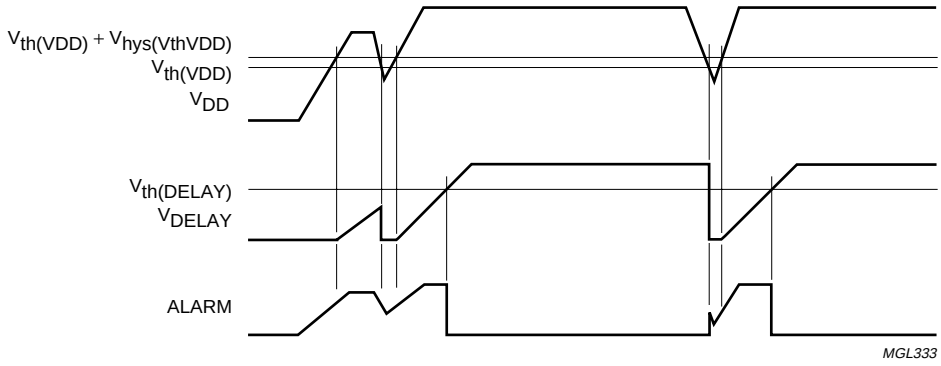


Fig.4 Supply supervisor.

Low impedance supply (pin LIS)

For some applications, it is mandatory that the contacts to the card (V_{CC}, RST, CLK and I/O) are low impedance while the card is inactive and also when the coupler is not powered. An auxiliary supply voltage on pin LIS ensures this condition where $I_{LIS} \leq 5$ µA for $V_{LIS} = 5$ V. This low impedance situation is disabled when V_{CC} starts rising during activation, and re-enabled when the step-up converter is stopped during deactivation. If this feature is not required, the LIS pin must be tied to V_{DDD}.

Step-up converter

Except for the V_{CC} generator and the other cards contacts buffers, the whole circuit is powered by V_{DDD} and V_{DDA}. If the supply voltage is 3 or 5 V, then a higher voltage is needed for the ISO contacts supply. When a card session is requested by the controller, the sequencer first starts the step-up converter, which is a switched capacitors type, clocked by an internal oscillator at a frequency of approximately 2.5 MHz. The output voltage $V_{step-up}$ is regulated at approximately 6.5 V and then fed to the V_{CC} generator. V_{CC} and DGND are used as a reference for all other cards contacts.

The step-up converter may be chosen as a doubler or a tripler by mask option, depending on the voltage and the current needed on the card.

ISO 7816 security

The correct sequence during activation and deactivation of the card is ensured through a specific sequencer, clocked by a division ratio of the internal oscillator.

Activation (START signal P05; see Table 3) is only possible if the card is present (PRES HIGH or LOW according to mask option), and if the supply voltage is correct (ALARM signal inactive); CLK and RST are controlled by RSTIN (internal signal; port P04), allowing the correct count of CLK pulses during answer-to-reset from the card.

The presence of the card is signalled to the controller by the OFF signal (port P10; see Table 3).

During a session, the sequencer performs an automatic emergency deactivation in the event of card take-off, supply voltage drop, or hardware problems. The OFF signal falls thereby warning the controller.

Clock circuitry

The clock to the microcontroller and the clock to the card are derived from the main clock signal (XTAL from 2 to 16 MHz, or an external clock signal).

Directly after reset and during power reduction modes the microcontroller clock frequency f_{clk} equals $\frac{1}{8}f_{INT}$; f_{INT} is always present because it is derived from the internal oscillator and gives the lowest power consumption. When required (for card session, serial communication or anything else) the microcontroller may choose to clock itself with $\frac{1}{2}f_{XTAL}$, $\frac{1}{4}f_{XTAL}$ or $\frac{1}{2}f_{INT}$. All frequency changes are synchronous, thereby ensuring no hang-up due to short spikes etc.

Cards clock: the microcontroller may select to send the card a card clock frequency of $\frac{1}{2}f_{XTAL}$, $\frac{1}{4}f_{XTAL}$, $\frac{1}{8}f_{XTAL}$ or $\frac{1}{2}f_{INT}$ (≈1.25 MHz), or to stop the clock HIGH or LOW. All transitions are synchronous, ensuring correct pulse length during start or change in accordance with ISO 7816.

After power on, CLK is set at STOP LOW and f_{clk} is set at $\frac{1}{8}f_{INT}$.

Power-down and sleep modes

The TDA8005A offers a large flexibility for defining power reduction modes by software. Some configurations are described below.

In the power-down mode, the microcontroller is in power-down and the supply and the internal oscillator are active. The card is not active; this is the smallest power consumption mode. Any change on P1 ports or on PRES will wake-up the circuit (for example, a key pressed on the keyboard, the card inserted or taken off).

In the sleep mode, the card is powered but configured in the idle or sleep mode. The step-up converter will only be active when it is necessary to reactivate $V_{step\text{-}up}$. When the microcontroller is in power-down mode any change on P1 ports or on PRES will wake up the circuit.

In both power reduction modes the sequencer is active, allowing automatic emergency deactivation in the event of card take-off, hardware problems, or supply dropout.

The TDA8005A is set into power-down or sleep mode by software. There are several ways to return to normal mode: insertion or extraction of the card, detection of a change on P1 (which can be a key pressed) or a command from the system microcontroller. For example, if the system monitors the clock signal on XTAL1, it may stop this clock after setting the device into power-down mode and then wake it up when sending the clock signal again. In this situation, the internal clock should have been used before the f_{clk}.

Peripheral interface

This block allows synchronous serial communication with the three peripherals (ISO 7816 UART, clock circuitry and output port extension); see Figs 1 and 5.

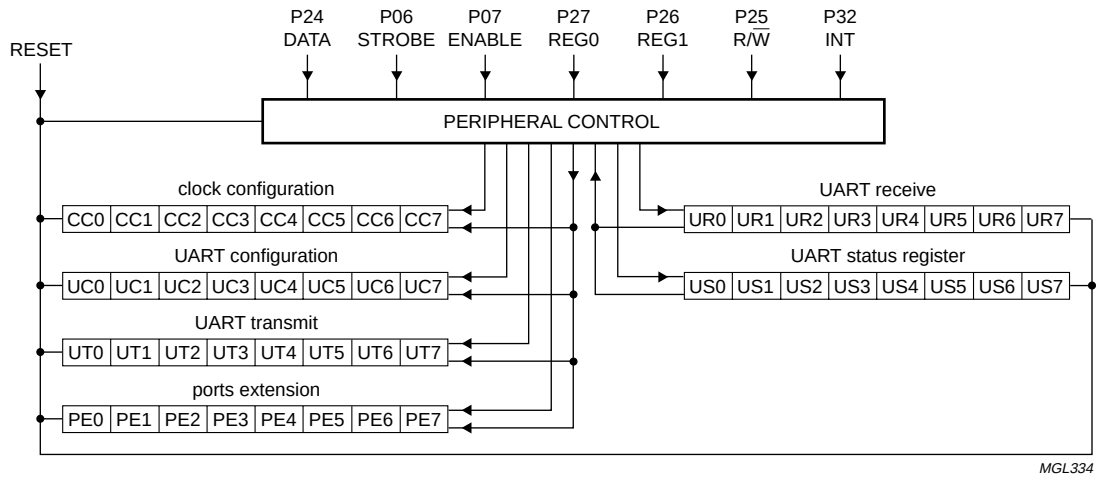


Fig.5 Peripheral interface diagram.

Table 2 Explanation of Fig.5; note 1

BIT NAME	DESCRIPTION
REG0 = 0, REG1 = 0 and R/$\overline{W}$ = 0; CLOCK configuration register (configuration after reset is cards clock STOP LOW, $f_{clk} = \frac{1}{8}f_{INT}$)	
CC0	cards clock = $\frac{1}{2}f_{XTAL}$
CC1	cards clock = $\frac{1}{4}f_{XTAL}$
CC2	cards clock = $\frac{1}{8}f_{XTAL}$
CC3	cards clock = $\frac{1}{2}f_{INT}$
CC4	cards clock = STOP HIGH
CC5	$f_{clk} = \frac{1}{2}f_{XTAL}$
CC6	$f_{clk} = \frac{1}{4}f_{XTAL}$
CC7	$f_{clk} = \frac{1}{2}f_{INT}$
REG0 = 1, REG1 = 0 and R/$\overline{W}$ = 0; UART configuration register (after reset all bits are cleared)	
UC0	ISO UART RESET
UC1	START SESSION
UC2	LCT (Last Character to Transmit)
UC3	TRANSMIT/RECEIVE
UC4	3 V/5 V
UC5 to UC7	not used
REG0 = 0, REG1 = 1 and R/$\overline{W}$ = 0; UART transmit register	
UT0 to UT7	LSB to MSB of the character to be transmitted to the card
REG0 = 1, REG1 = 1 and R/$\overline{W}$ = 0; PORTS EXTENSION (after reset all bits are cleared)	
PE0 to PE5	PE0 to PE5 is the inverse of the value to be written on K0 to K5
PE6 and PE7	not used
REG0 = 0, REG1 = 0 and R/$\overline{W}$ = 1; UART receive register	
UR0 to UR7	LSB to MSB of the character received from the card
REG0 = 1, REG1 = 0 and R/$\overline{W}$ = 1; UART status register (after reset all bits are cleared)	
US0	UART transmit buffer empty
US1	UART receive buffer full
US2	first start bit detected
US3	parity error detected during reception of a character (the UART has asked the card to repeat the character)
US4	parity error detected during transmission of a character; the controller must write the previous character in the UART transmit register, or abort the session
US5 to US7	not used

Note

1. All registers are active HIGH.

USE OF PERIPHERAL INTERFACE

Write operation

1. Select the correct register with R/$\overline{W}$, REG0 and REG1
2. Write the word in the Peripheral Shift Register (PSR) with DATA and STROBE; DATA is shifted on the rising edge of STROBE; 8 shifts are necessary
3. Give a negative pulse on ENABLE; the data is parallel loaded in the register on the falling edge of ENABLE.

Read operation

1. Select the correct register with R/$\overline{W}$, REG0 and REG1
2. Give a first negative pulse on ENABLE; the word is parallel loaded in the peripheral shift register on the rising edge of ENABLE
3. Give a second negative pulse on ENABLE for configuring the PSR in shift right mode
4. Read the word from PSR with DATA and STROBE; DATA is shifted on the rising edge of STROBE; 7 shifts are necessary.

EXAMPLE OF PERIPHERAL INTERFACE

```
;*************************************
;*CHANGE OF CLOCK CONFIGURATION REGISTER*
;*************************************
;
;**THE NEW CONFIGURATION IS SUPPOSED**
;**TO BE IN THE ACCUMULATOR**
             CLR REG0
             CLR REG1
             CLR R/W
             MOV R2,#8
LOOP         RRC A
             MOV DATA C
             CLR STROBE
             SET STROBE
             DJNZ R2,LOOP
             CLR ENABLE
             SET ENABLE
             SET DATA
             RET
```

```
;*************************************
;*READ CHARACTER ARRIVED IN UART RECEIVE*
;*****************REGISTER**************
;*************************************
;
;**THE CHARACTER WILL BE IN THE**
;**ACCUMULATOR**
             CLR REG0
             CLR REG1
             SET R/W
             CLR ENABLE
             SET ENABLE
             CLR ENABLE
             SET ENABLE
             MOV R2,#8
LOOP         MOV C,DATA
             RRC A
             CLR STROBE
             SET STROBE
             DJNZ R2,LOOP
             SET DATA
             RET
```

ISO UART

The ISO UART handles all the specific requirements defined in ISO T = 0 protocol type. It is clocked with the cards clock, which gives the $f_{clk}/31$ sampling rate for start bit detection (the start bit is detected at the first LOW level on I/O) and the $f_{clk}/372$ frequency for Elementary Time Unit (ETU) timing (in the reception mode the bit is sampled at $\frac{1}{2}$ETU). It also allows the cards clock frequency changes without interfering with the baud rate.

This hardware UART allows operating of the microcontroller at low frequency, thus lowering EM radiations and power consumption. It also frees the microcontroller of fastidious conversions and real time jobs thereby allowing the control of higher level tasks.

The following occurs in the reception mode (see Fig.6):

- Detection of the inverse or direct convention at the beginning of Answer To Reset (ATR)
- Automatic convention setting, so the microcontroller only receives characters in direct convention
- Parity checking and automatic request for character repetition in case of error (reception is possible at 12 ETU).

The following occurs in the transmission mode (see Fig.7):

- Transmission according to the convention detected during ATR, consequently the microcontroller only has to send characters in direct convention; transmission of the next character may start at 12 ETU in the event of no error or 13 ETU in case of error
- Parity calculation and detection of repetition request from the card in the event of error
- The bit LCT (Last Character to Transmit) allows fast reconfiguration for receiving the answer 12 ETU after the start bit of the last transmitted character.

The ISO UART status register can inform which event has caused an interrupt (buffer full, buffer empty, parity error detected etc.) in accordance with peripheral interface.

The register is reset when its status is read by the microcontroller.

The ISO UART configuration register enables the microcontroller to configure the ISO UART and to choose between 5 or 3 V cards. Bit UC4 (3 V/5 V) LOW means 5 V card, bit UC4 (3 V/5 V) HIGH means 3 V card; conform peripheral interface. The selection of 3 or 5 V card has to be done before activation.

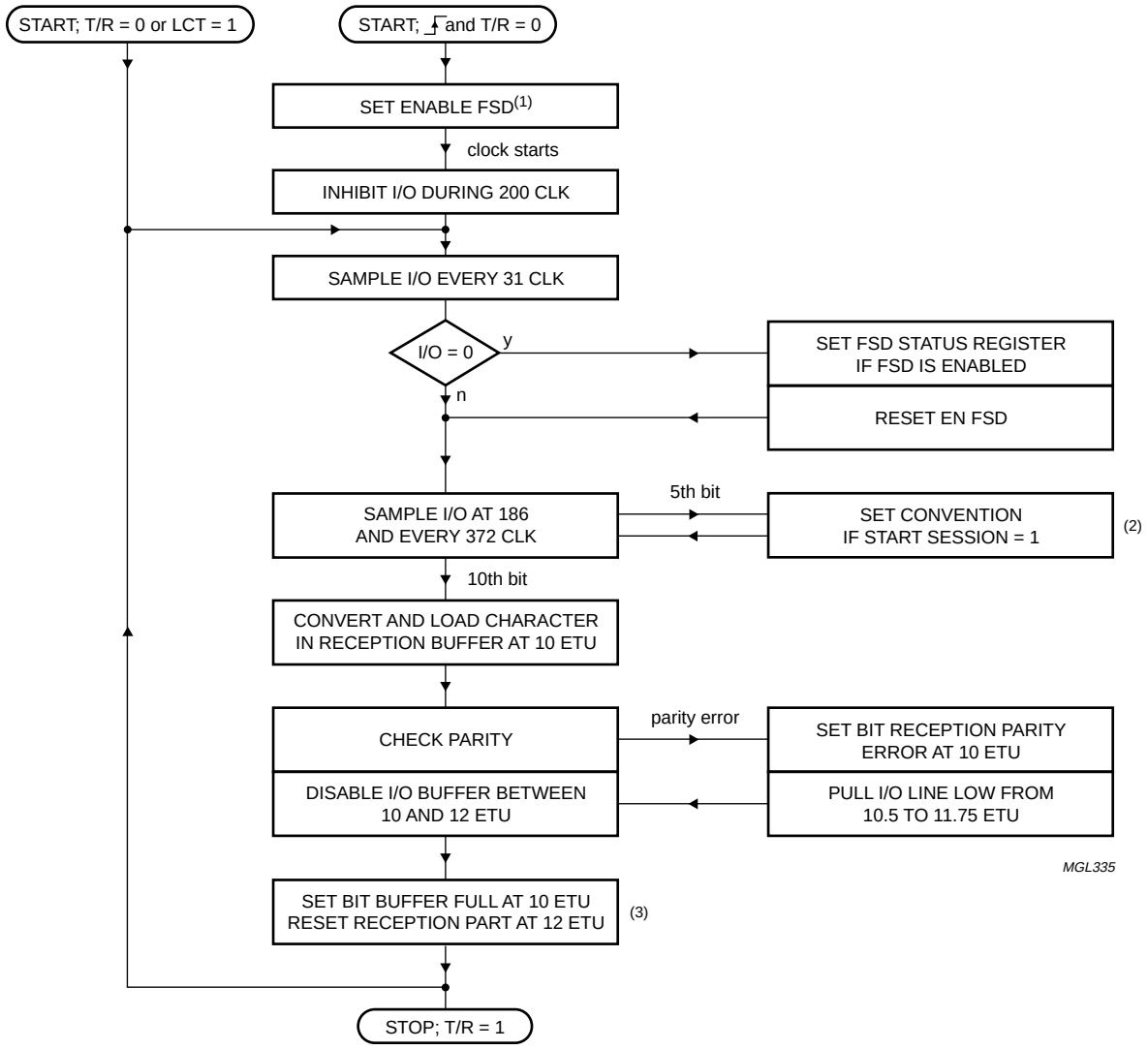
After power-on, all ISO UART registers are reset.

The ISO UART is configured in the reception mode. When the microcontroller wants to start a session, it sets the bits UC1 (START SESSION) and UC0 (ISO UART RESET) in the UART configuration register and then sets bit START SESSION LOW. When the first start bit on I/O is detected (sampling rate $f_{clk}/31$), the UART sets the bit US2 (first start bit detected) in the status register which gives an interrupt on internal port INT0 one clock pulse later.

The convention is recognized on the first character of the ATR and the UART configures itself in order to exchange direct data without parity processing with the microcontroller whatever the convention of the card is. Bit UC1 (START SESSION) must be reset by software. At the end of every character, the UART tests the parity and resets what is necessary for receiving another character.

If no parity error is detected, the UART sets bit US1 (UART receive buffer full) in the status register which warns the microcontroller it has to read the character before the reception of the next one has been completed. The status register is reset when read from the controller.

If a parity error has been detected, the UART pulls the I/O line LOW between 10.5 and 12 ETU. It also sets the bits US1 (UART receive buffer full) and US3 (parity error detected during reception of a character) in the status register which warns the microcontroller that an error has occurred. The card is supposed to repeat the previous character.



(1) FSD = First Start Detect.
(2) The start session is reset by software.
(3) The software may load the received character in the peripheral control at any time without any action on the ISO UART.

Fig.6 ISO UART reception flow chart.

When the controller needs to transmit data to the card, it first sets bit UC3 in the UART configuration register which configures the UART in the transmission mode. As soon as a character has been written in the UART transmit register, the UART makes the conversion, calculates the parity and starts the transmission on the rising edge of ENABLE. When the character has been transmitted, it surveys the I/O line at 11 ETU in order to know if an error has been detected by the card.

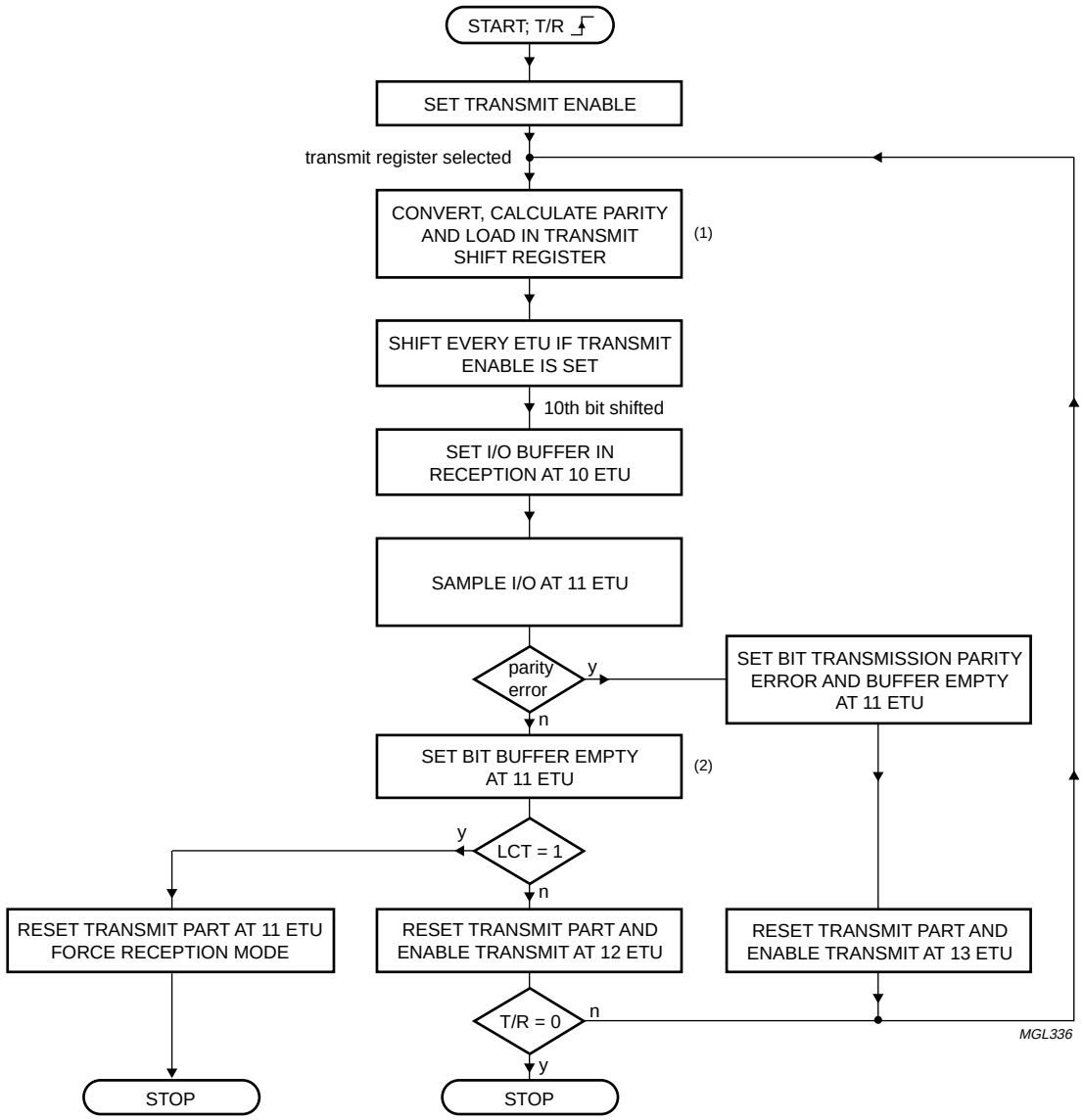
If no error has occurred, the UART sets bit US0 (UART transmit buffer empty) in the status register and waits for the next character. If the next character has been written before 12 ETU, the transmission will start at 12 ETU. If it was written after 12 ETU it will start on the rising edge of ENABLE.

If an error has occurred, it sets bits US0 and US4 (parity error detected during transmission of a character) which warns the microcontroller to rewrite the previous character in the UART transmit register.

If the character has been rewritten before 13 ETU, the transmission will start at 13 ETU. If it has been written after 13 ETU it will start on the rising edge of ENABLE.

When the transmission is completed, the microcontroller may set bit LCT (Last Character to Transmit) so that the UART will force the reception mode into ready to get the reply from the card at 12 ETU. This bit must be reset before the end of the first reception. Bit UC3 (TRANSMIT/RECEIVE) must be reset to enable the reception of the characters to follow.

When the session is completed, the microcontroller re-initializes the whole UART by resetting bit UC0 (ISO UART RESET).



(1) The transmit register may be loaded just after reading from the status register.

(2) The software must reset the last character but before completion of the first received character.

Fig.7 ISO UART transmission flow chart.

I/O buffer modes (see Fig.8)

The I/O buffer modes are:

- I/O buffer disabled
- I/O buffer in input, 20 kΩ pull-up resistor connected between I/O and V_{CC}, I/O masked till 200 clock pulses
- I/O buffer in input, 20 kΩ pull-up resistor connected between I/O and V_{CC}, I/O is sampled every 31 clock pulses
- I/O buffer in output, 20 kΩ pull-up resistor connected between I/O and V_{CC}
- I/O buffer in output, I/O is pulled LOW by the N transistor of the buffer
- I/O buffer in output, I/O is pulled HIGH or LOW by the P or N transistor.

Output ports extension

In the LQFP64 version, 6 auxiliary output ports may be used for low frequency tasks (for example, keyboard scanning). These ports are push-pull output types (in accordance with use in software document).

Activation sequence

When the card is inactive, V_{CC}, CLK, RST and I/O are LOW, with low impedance with respect to GND.
The step-up converter is stopped. The I/O is configured in the reception mode with a high impedance path to the ISO UART, subsequently no spurious pulse from the card during power-up will be taken into account until I/O is enabled. When conditions are fulfilled (supply voltage present, card present, no hardware problems), the microcontroller may initiate an activation sequence by setting START LOW (t_0; see Fig.9):

1. The step-up converter is started (t_1)
2. LIS signal is disabled by internal signal ENLI, and V_{CC} starts rising from 0 to 5 or 3 V (according to bit 4 of UART configuration register) with a controlled rise time of 0.1 V/µs typically (t_2)
3. I/O buffer is enabled (t_3)
4. Clock is sent to the card (t_4)
5. RST buffer is enabled (t_5).

In order to allow a precise count of clock pulses during ATR, a defined time window (t_3; t_5) is opened where the clock may be sent to the card by means of RSTIN (port P04). Beyond this window, RSTIN has no more action on clock, and only monitors the cards RST contact (RST is the inverse of RSTIN).

The sequencer is clocked by $f_{INT}/64$ which leads to a time interval T of 25 µs typical. Thus $t_1 = 0$ to $\frac{1}{64}T$, $t_2 = t_1 + \frac{3}{2}T$, $t_3 = t_1 + 4T$, $t_4 = t_3$ to t_5 and $t_5 = t_1 + 7T$.

Deactivation sequence

When the session is completed, the microcontroller sets START HIGH. The circuit then executes an automatic deactivation sequence (see Fig.10):

1. Card reset (RST falls LOW) at t_{10}
2. Clock is stopped at t_{11}
3. I/O becomes high impedance to the ISO UART (t_{12})
4. V_{CC} falls to 0 V with typical 0.1 V/µs slew rate (t_{13})
5. The step-up converter is stopped and CLK; RST, V_{CC} and I/O become low impedance to GND (t_{14})
6. $t_{10} < \frac{1}{64}T$; $t_{11} = t_{10} + \frac{1}{2}T$; $t_{12} = t_{10} + T$; $t_{13} = t_{10} + \frac{3}{2}T$; $t_{14} = t_{10} + 5T$.

Protections

Main hardware fault conditions are monitored by the circuit:

- Overcurrent on V_{CC} (in accordance with options as specified in Table 3)
- Short circuits between V_{CC} and other contacts
- Card take-off during transaction.

When one of these problems is detected, the security logic block pulls the interrupt line (port P10) OFF LOW, in order to warn the microcontroller and initiates an automatic deactivation of the contacts. When the deactivation has been completed, the OFF line returns HIGH, except if the problem was due to a card extraction in which case it remains LOW until a card is inserted.

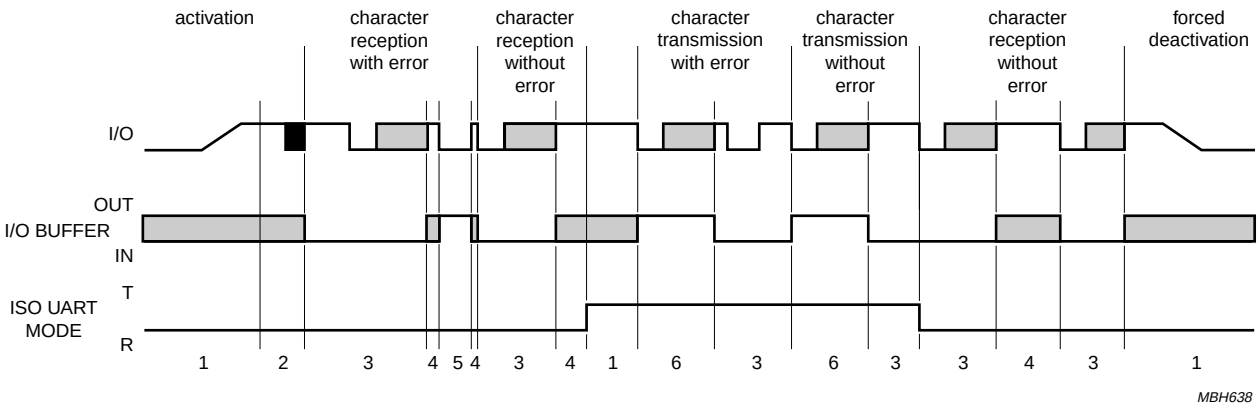


Fig.8 I/O buffer modes.

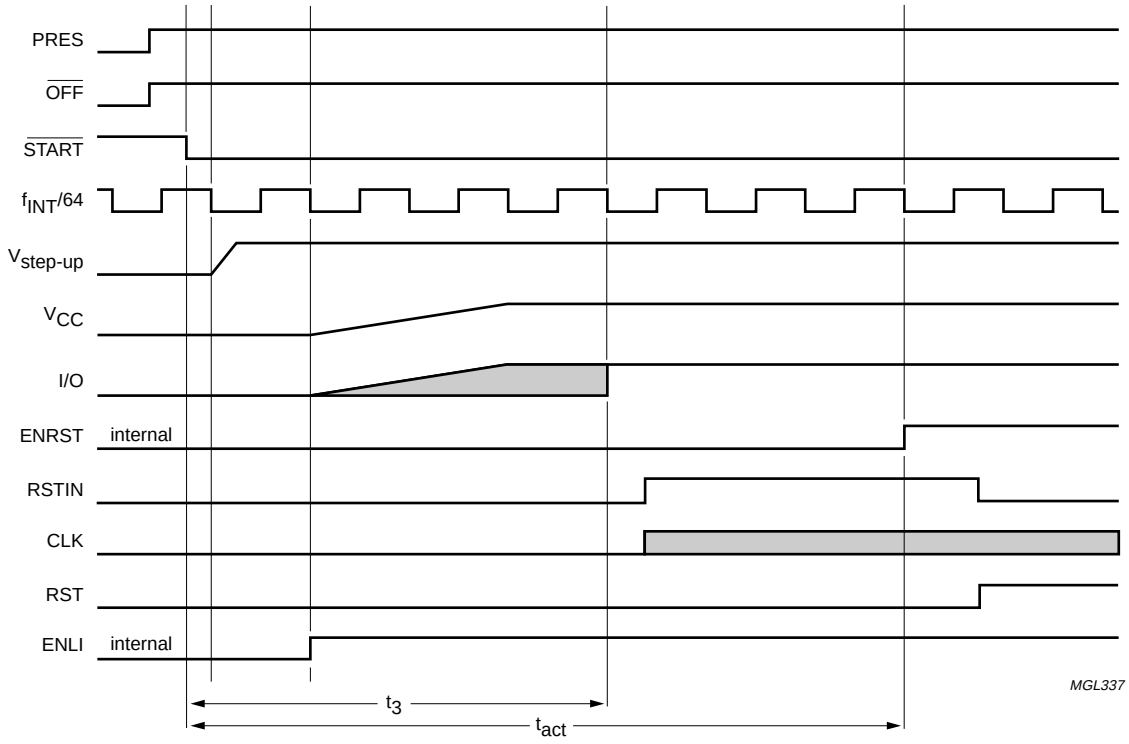


Fig.9 Activation sequence.

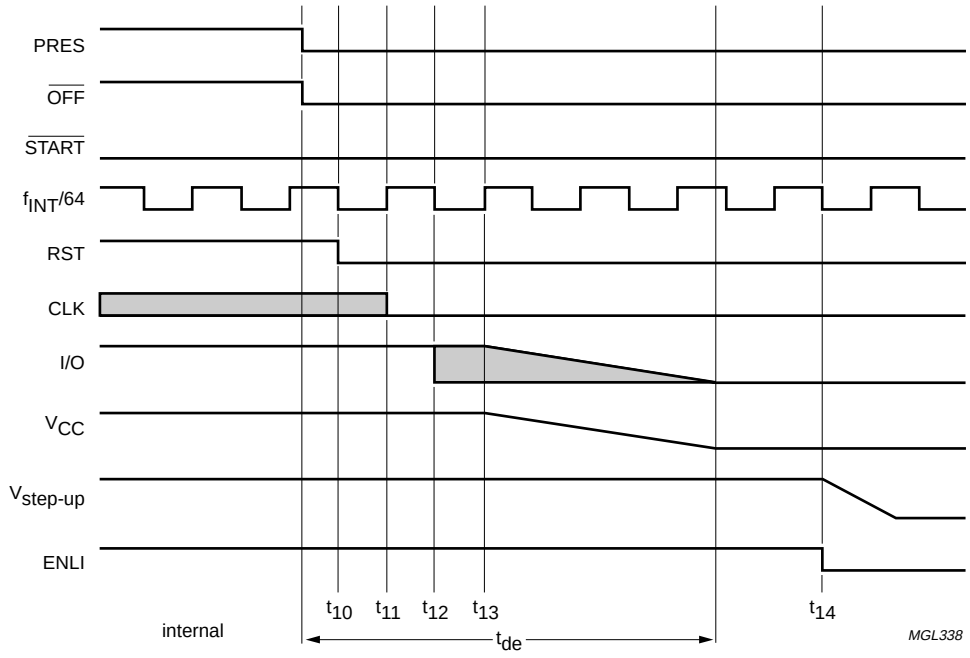


Fig.10 Emergency deactivation sequence after a card take-off.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage		–0.3	+6.5	V
V_{DDD}	digital supply voltage		–0.3	+6.5	V
V_n	all input voltages		–0.3	V_{DD} + 0.5	V
I_{n1}	DC current into pins XTAL1, XTAL2, RxD, TxD, RESET, INT1, T0 (port P34), P37, P00 to P03, P11 to P17, P20 to P23 and TEST1 to TEST4		–	5	mA
I_{n2}	DC current from or to pins AUX1 and AUX2		–10	+10	mA
I_{n3}	DC current from or to pins S1 to S5		–30	+30	mA
I_{n4}	DC current into pin DELAY		–5	+10	mA
I_{n5}	DC current from or to pin PRES		–5	+5	mA
I_{n6}	DC current from and to pins K0 to K5		–5	+5	mA
I_{n7}	DC current from or into pin ALARM (according to option choice)		–5	+5	mA
P_{tot}	total power dissipation	T_{amb} = –25 to +85°C	–	500	mW
T_{stg}	storage temperature		–55	+150	°C
V_{esd}	electrostatic discharge	on pins I/O, V_{CC}, RST, CLK and PRES	–6	+6	kV
		on other pins	–2	+2	kV
T_j	junction temperature	–	–	125	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	LQFP64		70	K/W
	QFP44		60	K/W

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; for general purpose I/O ports refer to P80CL51 data sheet; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	voltage superior, option dependant; note 1	2.5	–	6.0	V
$I_{DD(pd)}$	supply current in power-down mode	V_{DD} = 5 or 3 V; card inactive	–	100	–	µA
$I_{DD(sm)}$	supply current in sleep mode	card powered but clock stopped; no load				
		doubler option	–	500	–	µA
		tripler option	–	700	–	µA
$I_{DD(om)}$	supply current operating mode	unloaded; f_{XTAL} = 13 MHz; f_{clk} = 6.5 MHz; f_{card} = 3.25 MHz	–	5.5	–	mA
		V_{DD} = 3 V; f_{XTAL} = 13 MHz; f_{clk} = 3.25 MHz; f_{card} = 3.25 MHz	–	3	–	mA
$V_{th(VDD)}$	threshold voltage on V_{DD} (falling)	supervisor option	2	–	2.3	V
			2.45	–	3	V
			3.8	–	4.5	V
$V_{hys(VthVDD)}$	hysteresis on $V_{th(VDD)}$		40	–	350	mV
$V_{th(DELAY)}$	threshold voltage on pin DELAY		–	1.38	–	V
V_{DELAY}	voltage on pin DELAY		V_{DD} – 0.5	–	V_{DD}	V
I_{DELAY}	output current at pin DELAY	pin grounded (charge)	–1.5	–1	–0.4	µA
		V_{DELAY} = V_{DD} (discharge)	4	6.8	10	mA
t_W	ALARM pulse width	C_{DELAY} = 10 nF	–	10	–	ms
ALARM (open drain active HIGH or LOW output)						
I_{OH}	HIGH-level output current	active LOW option; V_{OH} = 5 V	–	–	10	µA
V_{OL}	LOW-level output voltage	active LOW option; I_{OL} = 2 mA	–	–	0.4	V
I_{OL}	LOW-level output current	active HIGH option; V_{OL} = 0 V	–	–	–10	µA
V_{OH}	HIGH-level output voltage	active HIGH option; I_{OH} = –2 mA	V_{DD} – 1	–	–	V
Crystal oscillator; note 2						
f_{XTAL}	crystal frequency		2	–	16	MHz
f_{ext}	frequency of external signal applied on pin XTAL1		0	–	16	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Step-up converter						
f_{INT}	internal oscillation frequency		2	–	3	MHz
$V_{step-up}$	voltage on pin S5	5 V card	–	6.5	–	V
		3 V card	–	4.5	–	V
Low impedance supply (pin LIS)						
V_{LIS}	voltage on pin LIS		0	–	V_{DD}	V
I_{LIS}	current at pin LIS		–	–	7	µA
Reset output to the card (pin RST)						
$V_{o(RST)}$	output voltage	when inactive or when LIS is used; $I_{o(RST)}$ = 1 mA	–0.3	–	+0.4	V
$I_{o(RST)}$	output current	when inactive and pin grounded	–	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	–0.25	–	+0.4	V
V_{OH}	HIGH-level output voltage	$I_{OH} \leq -200$ µA				
		5 V card	4	–	V_{CC} + 0.3	V
		3 V card	2.4	–	V_{CC} + 0.3	V
t_r	rise time	C_L = 30 pF	–	–	1	µs
t_f	fall time	C_L = 30 pF	–	–	1	µs
Clock output to the card (pin CLK)						
$V_{o(CLK)}$	output voltage	when inactive or when LIS is used; $I_{o(CLK)}$ = 1 mA	–0.3	–	+0.4	V
$I_{o(CLK)}$	output current	when inactive and pin grounded	–	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	–0.25	–	+0.4	V
V_{OH}	HIGH-level output voltage	$I_{OH} \leq -200$ µA	V_{CC} – 0.5	–	V_{CC} + 0.25	V
t_r	rise time	C_L = 30 pF	–	–	15	ns
t_f	fall time	C_L = 30 pF	–	–	15	ns
f_{clk}	clock frequency	1 MHz idle configuration	1	–	1.5	MHz
		low operating speed	–	–	2	MHz
		middle operating speed	–	–	4	MHz
		high operating speed	–	–	8	MHz
δ	duty cycle	C_L = 30 pF	45	–	55	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Card supply voltage (pin V_{CC})						
$V_{o(VCC)}$	card supply output voltage	when inactive and when LIS is used; $I_{o(VCC)}$ = 1 mA	–0.3	–	+0.4	V
		when active; 5 V card				
		no load	4.85	5.05	5.25	V
		static load	4.75	5.0	5.25	V
		dynamic loads on 200 nF capacitor	4.5	–	5.4	V
		when active; 3 V card				
		no load	2.9	3.03	3.15	V
		static load	2.79	3	3.21	V
		dynamic loads on 200 nF capacitor	2.75	–	3.25	V
$I_{o(VCC)}$	card supply output current	when inactive and pin grounded	–	–	–1	mA
		when active	–	–	20	mA
		limited	–	–	note 1	mA
SR	slew rate on V_{CC} (rise and fall)	maximum load capacitor 250 nF (including typical 200 nF decoupling)	0.04	0.1	0.16	V/µs
Data line (pin I/O)						
$V_{o(I/O)}$	output voltage	when inactive or when LIS is used; $I_{o(I/O)}$ = 1 mA	–0.3	–	+0.4	V
$I_{o(I/O)}$	output current	when inactive and pin grounded	–	–	–1	mA
V_{OL}	LOW-level output voltage	I/O configured as output; I_{OL} = 1 mA	–0.25	–	+0.3	V
V_{OH}	HIGH-level output voltage	I/O configured as output; $I_{OH} \leq 100$ µA	$0.8V_{CC}$	–	V_{CC} + 0.25	V
V_{IL}	LOW-level input voltage	I/O configured as input; I_{IL} = 1 mA	0	–	0.5	V
V_{IH}	HIGH-level input voltage	I/O configured as input; I_{IL} = 100 µA	$0.6V_{CC}$	–	V_{CC}	V
t_r	rise time	C_L = 30 pF	–	–	1	µs
t_f	fall time	C_L = 30 pF	–	–	1	µs
Protections						
$I_{CC(sd)}$	shutdown current at pin V_{CC}		–	00/30/60; note 1	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
t_{act}	activation sequence duration		–	–	225	µs
t_{de}	deactivation sequence duration		–	–	150	µs
$t_{3(start)}$	start of the window for sending clock to the card		–	–	130	µs
$t_{5(end)}$	end of the window for sending clock to the card		140	–	–	µs
Auxiliary outputs (AUX1 and AUX2)						
V_{OL}	LOW-level output voltage	I_{OL} = 5 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –5 mA	V_{DD} – 1	–	–	V
Output ports from extension (K0 to K5)						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA	V_{DD} – 1	–	–	V
Card presence input (pin PRES)						
V_{IL}	LOW-level input voltage	I_{IL} = –1 mA	–	–	0.6	V
V_{IH}	HIGH-level input voltage	I_{IH} = 100 µA	$0.7V_{DD}$	–	–	V
I_{IH}	HIGH-level input current	V_{IH} = 5 V	0.2	–	3	µA

Notes

1. See Table 3 for mask options.
2. The crystal oscillator is the same as option 3 of the P80CL51.

APPLICATION INFORMATION

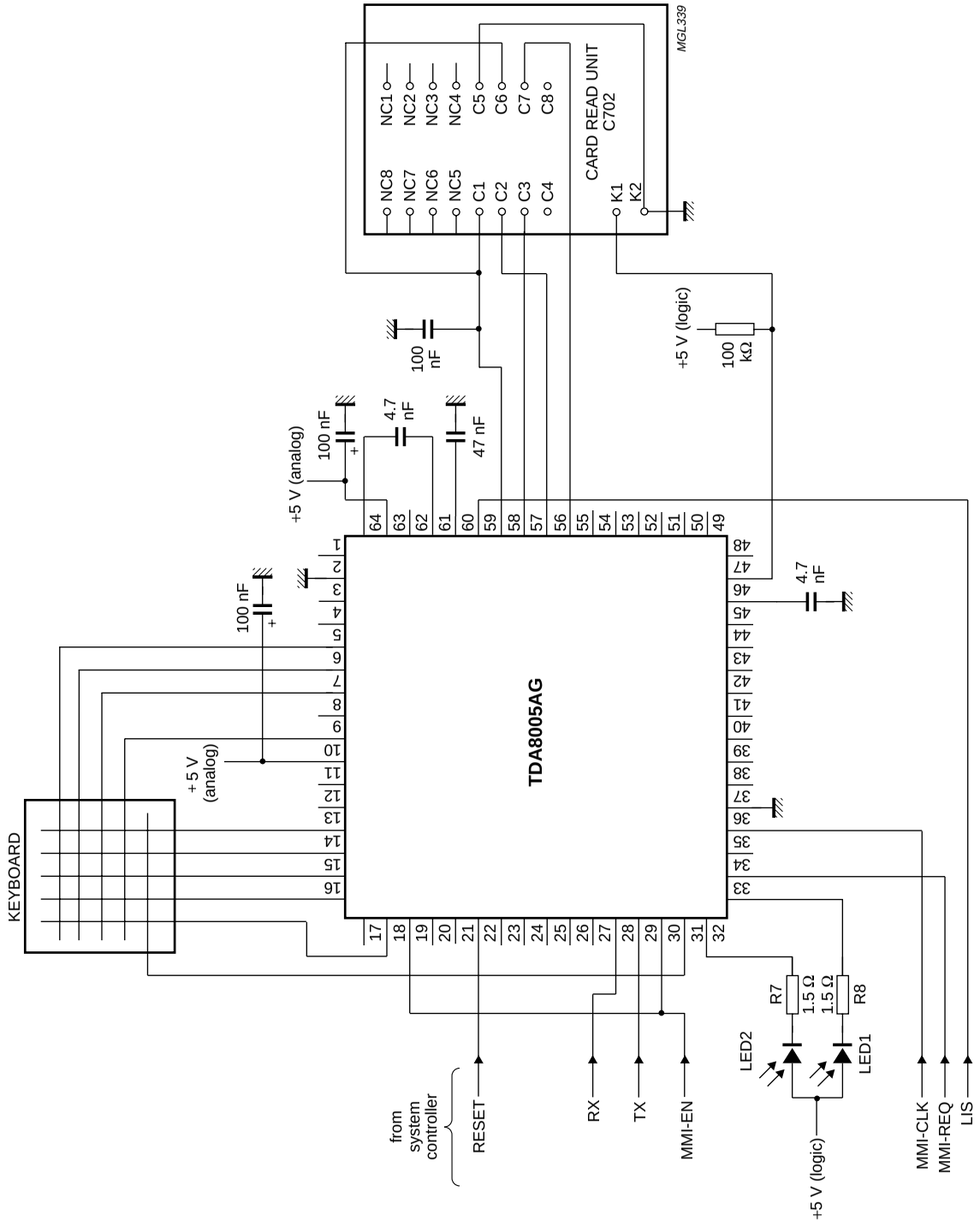


Fig.11 Possible GSM application.

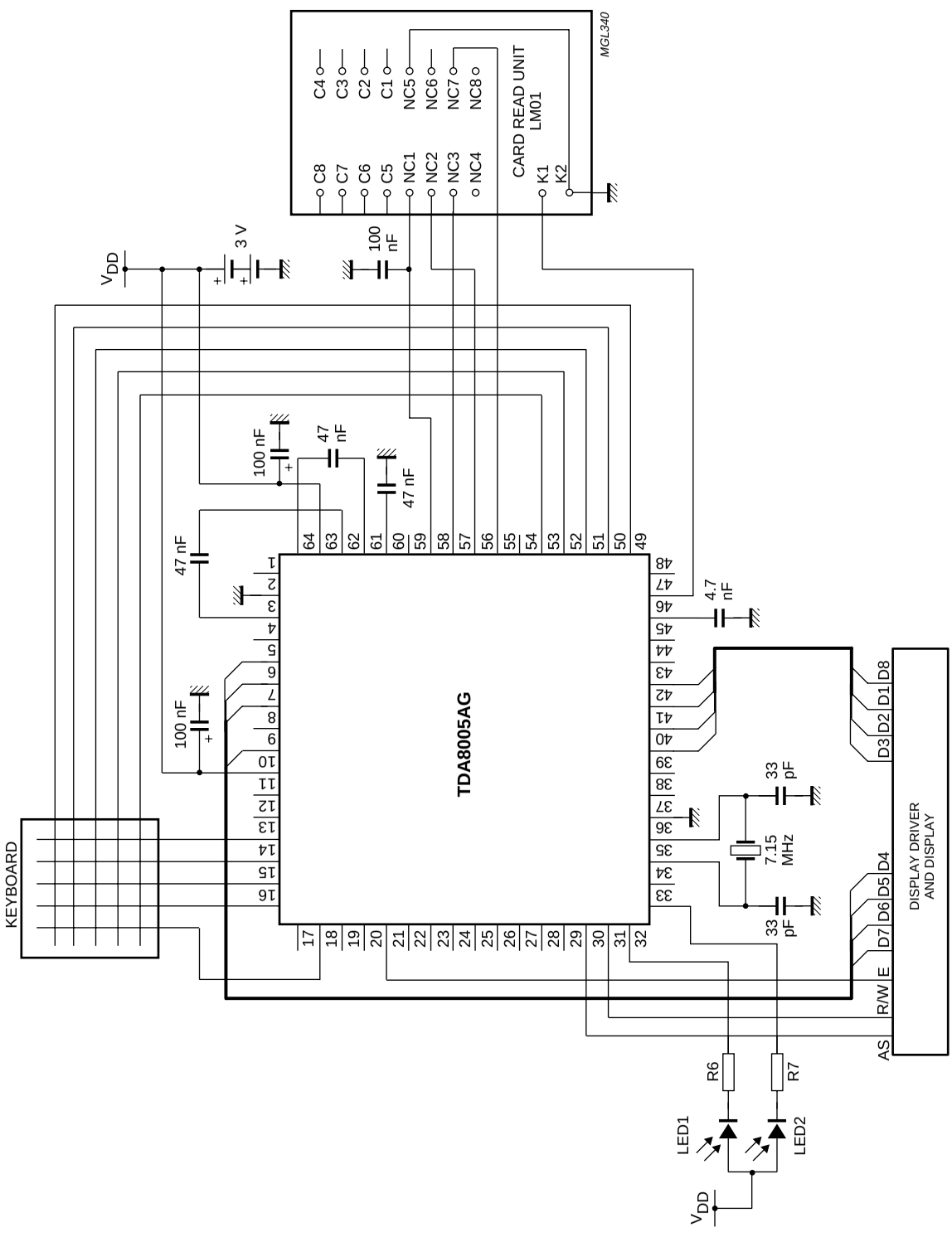


Fig.12 Possible stand-alone application.

Mask options

Table 3 TDA8005A option choice form

FUNCTION	DESCRIPTION	OPTION
P00		
P01		
P02		
P03		
P04	RSTIN	3 S
P05	START	3 S
P06	STROBE	3 S
P07	ENABLE	3 S
P10	OFF	2 S
P11		
P12		
P13		
P14		
P15		
P16		
P17		
P20		
P21		
P22		
P23		
P24	DATA	1 S
P25	R/$\overline{W}$	3 S
P26	REG1	3 S
P27	REG0	3 S
P30		
P31		
P32	INT	1 S
P33		
P34		
P35	AUX1	3 S
P36	AUX2	3 S
P37		

Table 4 Description of used options; note 1

OPTION	DESCRIPTION
1	standard I/O
2	open-drain I/O
3	push-pull output
S	set to HIGH state
R	set to LOW state

Note

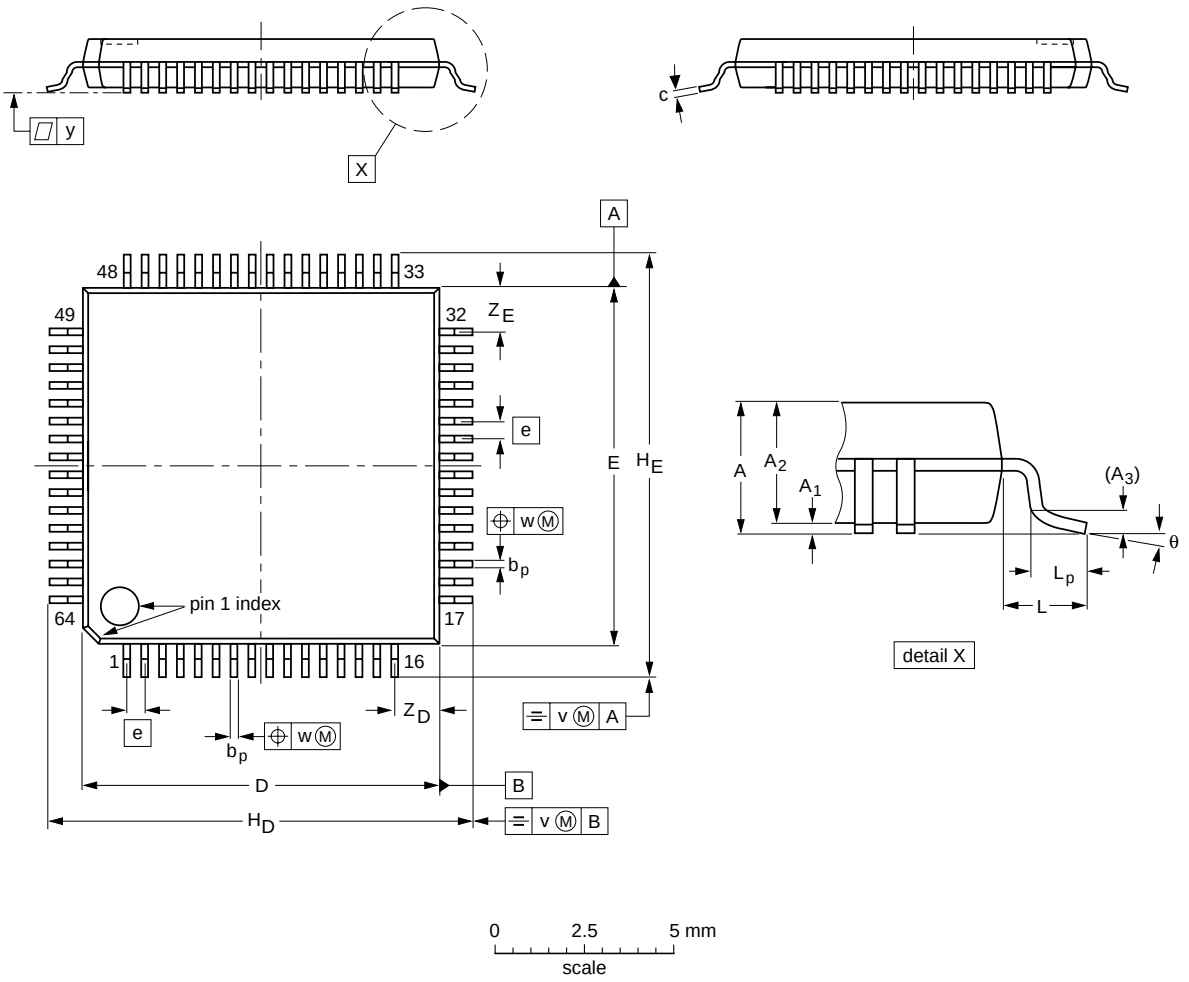
1. Example: option 1 S indicates standard I/O, set to HIGH state at power-on.

Table 5 Analog options

FEATURES	OPTIONS			
Step-up	doubler	tripler		
Supervisor	2.3 V	3 V	4.5 V	
I/O	low	high impedance		
I/O pull-up	10 kΩ	20 kΩ	30 kΩ	
R-CLK	0	100 Ω	150 Ω	200 Ω
R-RST	0	80 Ω	130 Ω	180 Ω
ALARM	active HIGH	active LOW		
PRES	active HIGH	active LOW		
IC protection	no limitation	30 mA limitation	60 mA limitation	

PACKAGE OUTLINES

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

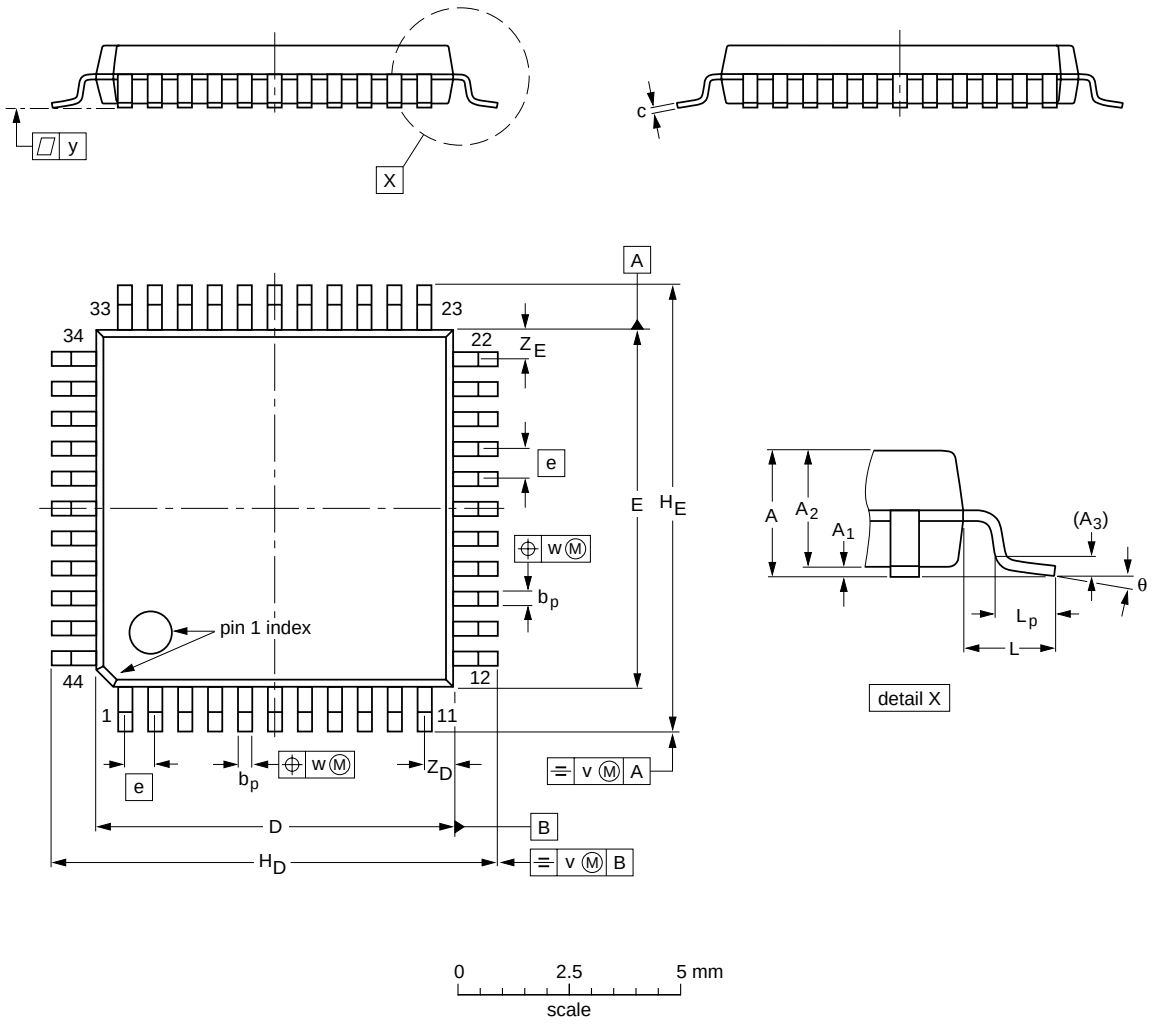
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2						~~95-12-19~~ 97-08-01

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP and QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP and QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all LQFP and QFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for LQFP and QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

NOTES

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